Supplementary Informations to Microwave surface transport in narrow-bandgap $PdSe_2$-MOSFETs

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Supplementary Section 1: Raman characterization

Figure 1 represents the experimental $PdSe_2$ Raman spectra of the S43 MOSFET channel (panel (a)), and of the S02 2D-FET channel (panel (b)). Analysis of the samples by Raman spectroscopy was carried out on a Renishaw Invia confocal microscopy system using a 633nm (red lines) and a 532nm (green lines) excitation lines.

The characteristic Raman signatures of orthorhombic $PdSe_2$ are clearly observed, in perfect agreement with the literature.[1,2] We observe the standard signature of $PdSe_2$ thinness in the ratio of the A_g^1/A_g^3 which is lower for the thin channel device.

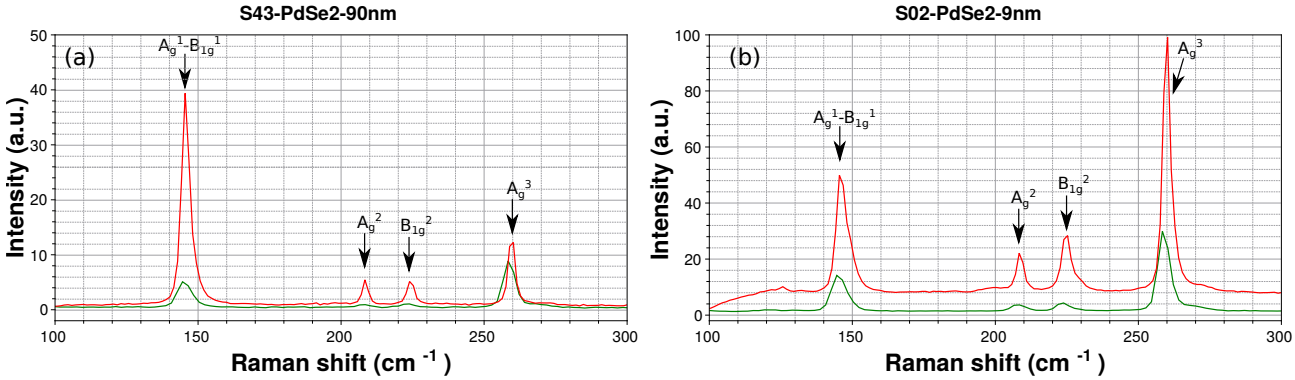

FIG. 1: Raman spectra of the thick PdSe2 transistor (panel (a)) and thin PdSe2 transistor (panel (b)), for a 633nm excitation line (red line) and a 532nm excitation line (green line). The Raman peaks are labeled by the corresponding Raman-active vibrational modes.

Supplementary Section 2: overview of room-temperature $PdSe_2$ transistors transfer characteristics

In order to assess the reproducibility of $PdSe_2$ transistor characteristics, we show in figures 2 the room-temperature transfer characteristics of the ten $PdSe_2$ devices investigated in this study, measured under vacuum and obscurity with a drain bias $V_{ds} < 50$mV. We have separated the thin and thick channel devices in panels (a) and (b) respectively. As seen in the figures, samples S02 (panel (a)) and S43 (panel (b) and (c)) - which are extensively analyzed in the main text - are representative of the two series. We also report in Table I their corresponding geometrical dimensions.

Contrary to thick channel devices (panel (b)), thin-channel devices (panel (a)) are characterized by a larger resistance dynamics and a larger sample-to-sample variability. In the following, we concentrate on thick-channel MOSFET devices which is the focus of our study.

Thick-channel transistors (MOSFETs) display quite similar transfer characteristics with a sharp resistance maximum close to gate charge neutrality ($V_G = -2$;–+2 V), limited by bulk conduction, and ambipolar transport in the surface layer with, however, a larger mobility for n-type doping. In order to assess the surface layer property, we plot in panel (c) the square resistance $R_\square(V_G)$, which turns out to compensate for most of the sample-to-sample dispersion (except for sample S01).

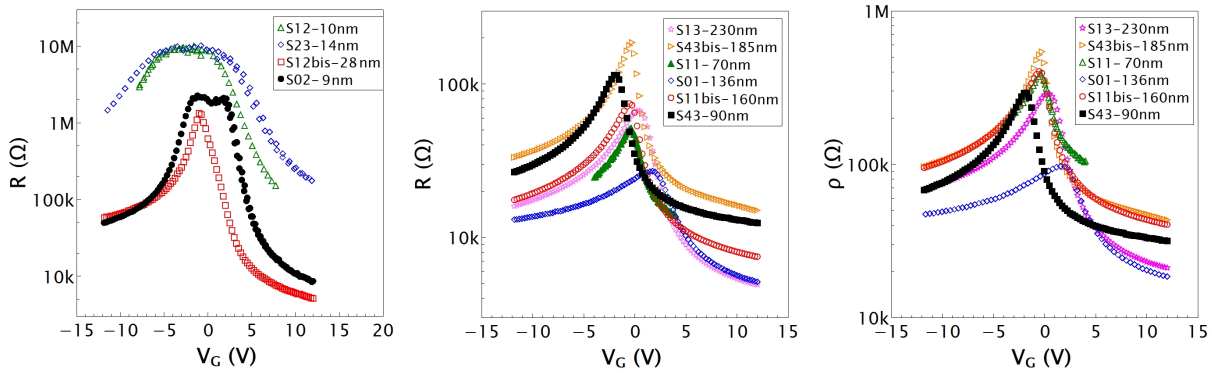

FIG. 2: Room temperature transfer characteristics of $PdSe_2$ transistors. Panel (a) corresponds to the thin-channel transistors, referred to as $PdSe_2$ 2D-FETS in the main text; Panel (b) corresponds to thick-channel transistors, referred to as $PdSe_2$-MOSFETs in the main text. Panel (c) is a replot of Panel (b) data in terms of in plane square resistance. Representative Samples S43 and S02, detailed in the main text, are highlighted as filled black symbols.

Finally, let us consider more in detail the classification of $PdSe_2$ FETs according to their thicknesses: S12bis is an emblematic example in this regard. In figure 2.a, it is classified as a "thin" transistor. However, with its channel thickness of 28nm, it lies at the limit between the "thick" and the "thin" FETs, and has an in-between behaviour as revealed by its transfer curves for various temperatures shown on Figure 3. We note a larger on/off ratio compared to "thick" FETs, due to a reduced intrinsic carriers contribution from the bulk. At low temperature ($T = 180$K), we note a moderate rise of the Schottky contact for n-type doping whereas, above ambient temperature, we do not observe the contact resistance

Sample name	Length (μm)	Width (μm)	$PdSe_2$ thickness (nm)	hBN thickness (nm)
S01	9.5	34.5	136	29
S02	**2.8**	**13.2**	**9**	**47**
S11	6.2	33.5	70	40
S11bis	9.5	71	160	60
S12	5.5	5.8	10	15
S12bis	9.5	20.4	28	29
S13	10	43	230	48
S23	3.2	4.6	14	37
S43	**10**	**25.5**	**90**	**34**
S43bis	10	29	185	29

TABLE I: Geometrical dimensions of the ten $PdSe_2$ transistors used in this study. The transistors presented in the main text are indicated in bold font.

contributions.

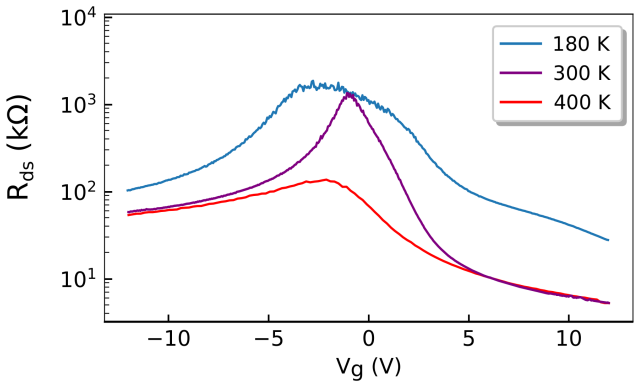

FIG. 3: Transfer characteristics of a PdSe2 FET with intermediate thickness (S12bis, 28nm) at various temperatures.

Supplementary Section 3: Schottky barrier height and channel resistance analyses of RF admittance spectra

The full RF modelization of the S43 FET allows accessing simultaneously the channel resistance and the Schottky junction one. In this supplementary information, we show the consistency of our analysis by performing the channel resistance and the Schottky contact analyses that are described in section III of the main text, but by using the RF-deembedded contact and channel resistances from the analysis of section IV, instead of the DC total transistor resistance that have required hypotheses on the relative importance of contact and channel resistance with respect to the doping. As we shall see, we recover results consistent with both DC and RF analyses.

Figure 4 represents the deembedded Schottky contact resistance (panel (a)) and channel resistance (panel (b)) function of gate voltage for various temperatures.

The Schottky barrier height deduced from panel (a) is represented on panel (c). It directly corresponds to the DC analysis of the inset of figure 1 (c) and likewise allows deducing a bandgap value of $E_g = 150 \pm 10$meV.

The deembedded channel resistance of figure 4 panel (b) is used to evaluate the activation energy of transport by intrinsic carrier and is represented on Figure 4 (d). When the Fermi level lies in the middle of the gap, the corresponding activation energy is equivalent to half of the bandgap energy. For this analysis, the temperature range is limited to $237 - 300$K so as to ensure that the transistor RF response is correctly modeled by the distributed line model, as discussed in section 4. From this analysis, we infer a bandgap value of $E_g = 160 \pm 20$meV.

Supplementary Section 4: Admittance spectra compilation

The supplementary videos are compilations of RF admittance spectra for all the gate bias points at T=176K and T=294K, respectively. The displayed curves correspond to the raw measurements of the real (red) and imaginary (light blue) parts of the Y12 parameters. Due to the parasitic contribution of the drain-gate capacitance (significant as contacts are deposited on a gated channel), another representation of the imaginary part of Y12, de-embedded from this parasitic capacitive coupling, is provided in dark blue (and is the one shown in the figure 2 of the main text). While both raw and de-embedded imaginary

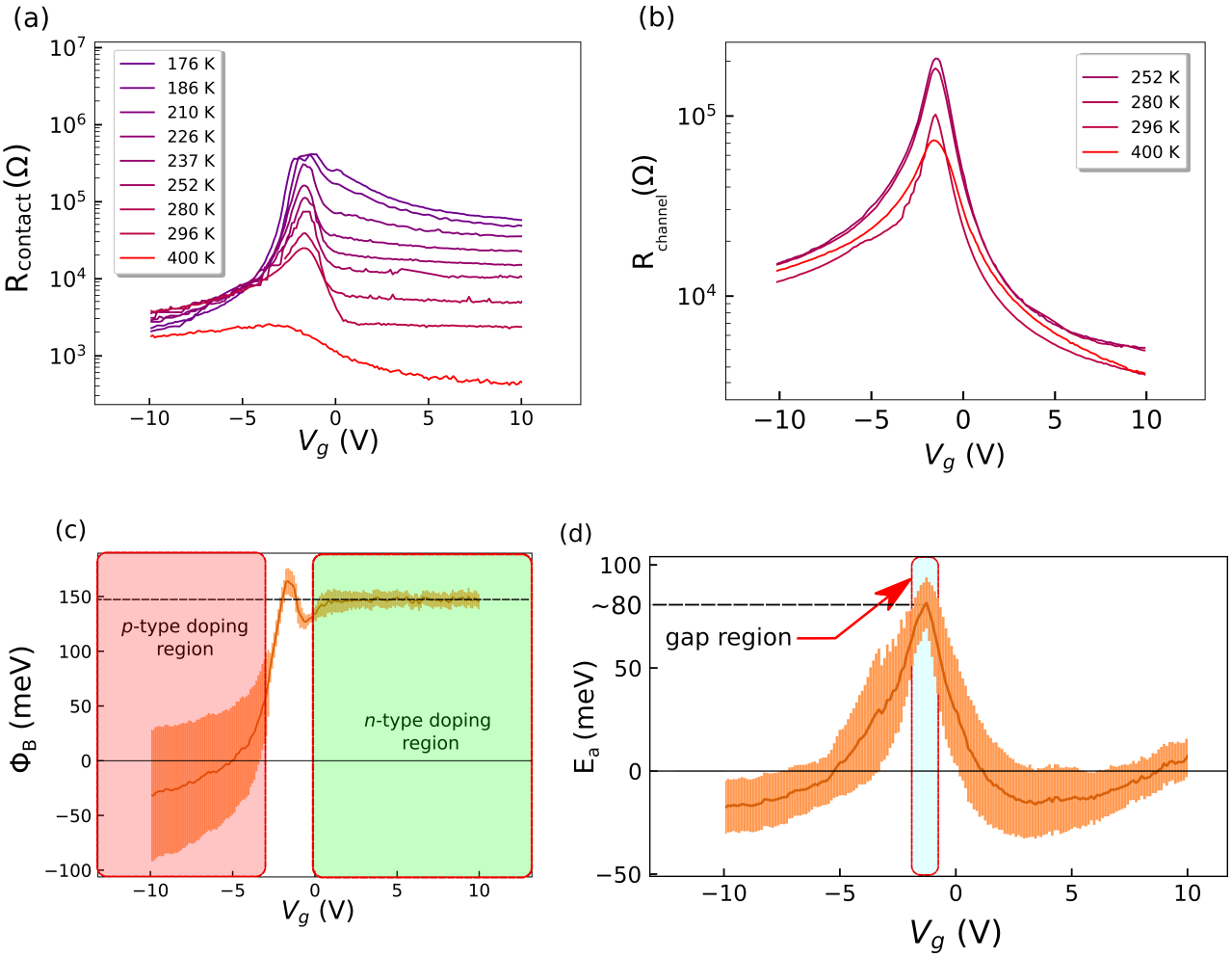

FIG. 4: Schottky barrier height and channel resistance analyses of RF admittance spectra. Deembedded contact resistance (a) and channel resistance (b) from the modeling of RF admittance spectra at various temperatures. (c) Extracted Schottky barrier height from the temperature behavior of Schottky barrier resistance (panel (a)). (d) Extracted activation energy from the temperature behavior of the channel resistance in panel (b).

parts almost overlap each other at low frequencies, above the channel cut-off frequency, the parasitic capacitive contribution (proportional to ω) overwhelms the one of the channel in the evanescent regime (proportional to $\sqrt{\omega}$). This occurs despite the relatively small contact surface compared to the channel surface.

For each RF admittance spectrum, the complex admittance parameter Y12 is fitted thanks to the theoretical expression (2) in the main text (taking into account the drain-gate capacitance), which allows the full extraction of the MISFET electrokinetic parameters

(r,c_g,C_{Schottky}, G_{Schottky}). Figure 2 gathers spectra for three emblematic gate biases (one for p-doped channel, another for depleted channel and the last one for n-doped channel).

The videos reveal a fine agreement, for all the bias points, between data and the adjusted model fits for T=294K, and for T=176K except in the $[-2.3; -0.1]$ V gate-bias blind region where the model no longer follows the data. As discussed in the main text, this fitting failure is caused by the channel cut-off frequency falling below the useful frequency range of the VNA, precluding reliable parameter adjustment of the model.

Bibliography

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[1] A. D. Oyedele, S. Yang, L. Liang, A.A. Puretzky, K. Wang, J. Zhang, P. Yu, P.R. Pudasaini, A.W. Ghosh, Z. Liu, C.M. Rouleau, B.G. Sumpter, M.F. Chisholm, W. Zhou, P.D. Rack, D.B. Geohegan, K. Xiao, *J. Am. Chem. Soc.* **139**, 14090 (2017). *PdSe2: Pentagonal Two-Dimensional Layers with High Air Stability for Electronics*

[2] W. L. Chow, P. Yu, F. Liu, J. Hong, X. Wang, Q. Zeng, C-H. Hsu, C. Zhu, J. Zhou, X. Wang, J. Xia, J. Yan, Y. Chen, D. Wu, T. Yu, Z. Shen, H. Lin, C. Jin, B. K. Tay, Z. Liu, *Adv. Mater.* **29**, 1602969 (2017). *High Mobility 2D Palladium Diselenide Field-Effect Transistors with Tunable Ambipolar Characteristics.*