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To cite this article before publication: Romaric Le Goff et al 2021 2D Mater. in press https://doi.org/10.1088/2053-1583/abfe9f

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Microwave surface transport in narrow-bandgap PdSe₂-MOSFETs

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Abstract

Group-10 transition-metal dichalcogenides are puckered van der Waals semiconductors, with a narrow bandgap, envisioned for ultra-broadband infrared detection. To assess their dynamical transport properties we investigate PdSe₂ n-MOSFETs by using microwave gate-capacitance spectroscopy. We report on surface channel inversion-depletion-accumulation behaviors with a depletion length of 15 nm, a mobility of 110 cm²V⁻¹s⁻¹, and a bulk bandgap of 0.15 eV. Our ten-micrometer-long devices have an electronic cutoff-frequency in the GHz range promising a large gain-bandwidth product, competitive with that of III-V (InAs) and II-VI (HgCdTe) devices. The integration of bulk absorption and surface readout in PdSe₂-MOSFETs is a monolithic geometry suitable for fast infrared detection in the application-rich 1–10 μ m range, which includes molecular spectroscopy, atmospheric communications and thermal sensing.

I. INTRODUCTION

Beyond the mostly investigated group-6 transition-metal dichalcogenides (TMDs: MoS_2 , MoSe₂, WSe₂) [1,2], noble-metal-based group-10 TMDs (PtSe₂, PdSe₂, PdTe₂) have recently attracted attention due to their high carrier mobility and thickness-dependent bandgap, inherited from their puckered 2D pentagonal structure [3]. As a representing member, $PdSe_2$ is air-stable, easily exfoliated, and theoretically possesses an indirect bandgap of 1.3 eV in single layers that vanishes in few-layers and bulk crystals [4–6]. The transport band gap of bulk PdSe₂ is largely unknown experimentally while predicted to be smaller or on the order of 0.2 eV [4,6]. With respect to 3D semiconductors used for IR detection, bandgap is smaller than that of InAs (0.354 eV) and comparable with that of HgCdTe ternary alloys (0.1–0.3 eV). Among van der Waals materials, PdSe₂ photo-transistors can be regarded as semiconducting alternatives to semimetallic graphene photodetectors [7], including mid-infrared photo-transistors [8] and near-infrared photo-mixers [9]. The predicted $PdSe_2$ bandgap is demarcated by a valence band whose maximum lies at the Γ point, and a conduction band whose minimum lies in the vicinity of the S point, both bands are characterized by an effective mass $m_e^* \sim 0.2m_0$ [10]. Alike PtSe₂ [11] or PdTe₂ [12] phototransistors, few-layer PdSe₂ field-effect transistors (FETs) have been investigated, showing a large mobility $\mu > 100 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [4,5], and a broadband photoresponse from visible to the near infrared (NIR) range [13,14]. Remarkably, the photoresponse can be extended to the long-wavelength mid-infrared (MIR) range in quasi-bulk samples [15,16]. PdSe₂ mobility remains impurity limited and likely to improve with progress in material growth up to phonon-limited values [10]. Large among TMDs, it cannot surpass that of narrow bandgap semiconductors ($\sim 30000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ in Ref.[17]). We show here that it is sufficient to secure a GHz electronic response. The ultra broadband optical gain, in the wavelength range 0.4- μ m [15,16], and the large NIR gain $G_{NIR} \sim 700$ A/W [15], when combined with a large electronic bandwidth, are assets of bulk PdSe₂ photo-transistors. In this work, we provide a comprehensive study of electronic transport of PdSe₂ transistors.

Specifications for a fast and broadband infrared photo-transistor include: a narrow band gap material of sufficient thickness, wavelength compatible device dimensions, and a fast photo carrier collection and detection. High-mobility MOSFETs fulfill these constrains in combining a quasi-intrinsic bulk absorption with an efficient charge collection in the sur-

Page 3 of 17

face layer followed by a fast diffusion to the contacts. The latter mechanism limits their electronic cut-off frequency and photo-detection speed. We study Metal-hBN-PdSe₂ transistors. Due to bulk screening, DC transport in thick $PdSe_2$ (thickness $t_{PdSe_2} \gtrsim 100$ nm) is qualitatively different from that of few layers conventional (unscreened) PdSe₂ 2D-FET devices $(t_{\rm PdSe_2} \lesssim 20 \text{ nm})$ with a conductivity that vanishes in the bandgap. The thick PdSe₂ transistors are candidate MOSFETs⁴¹ which are van der Waals variants of conventional 3D semiconducting MOSFETs with a surface-layer dominated transport [17], and a semiconducting bulk. Compared to conventional few layer PdSe₂ 2D-FETs, PdSe₂ MOS-FETs benefit both from the more efficient absorption of incoming light by the bulk material, and from the natural protection of the conducting buried surface layer from the environment. In this letter we focus on the low-bias electronic characterization of bulk PdSe₂-MOSFETs, equipped with low Schottky-barrier Pd contacts [18], and compare them with few-layer transistors. PdSe₂-MOSFETs exhibit the characteristic surface inversiondepletion-accumulation regimes, as well as Schottky-contacts in the (n-doped) accumulation regime. From the thermal-activation analysis of the bulk conductance at surface depletion and of the Schottky-barrier (SB) resistance, we obtain two consistent estimates, $\Delta_{bulk} = 0.14 \pm 0.01 \text{ eV}$ and $\Delta_{SB} = 0.15 \pm 0.01 \text{ eV}$, of PdSe₂-MOSFET transport bandgap. These estimates contrast with the band gap value reported by literature ($\Delta_{bulk} \simeq 0.5 \text{ eV}$) [5,13], essentially based on optical techniques, presaging dominant photon absorption mechanisms different from the indirect fundamental electronic band gap absorption. Dynamical transport properties are characterized by gate-source admittance spectroscopy, which is a broad-band (100kHz-10GHz) variant of standard semiconductor gate capacitance techniques [18]. Note that high-frequency characterization of PdSe₂-FETs is precluded by the large channel resistance. Thanks to efficient SB (and geometrical) capacitive coupling, microwave measurements allow overcoming SB-resistance and revealing the ambipolar channel conductance and field-effect gate capacitance of PdSe₂-MOSFETs as function of doping and temperature. The resistance-peak gate voltage V_{CNP} indicates a small bulk n-doping, corresponding to a donor density $N_D \lesssim 10^{17} \text{ cm}^{-3}$, presumably due to residual Se vacancies, which is a general trend in the literature on dichalcogenides. [19] However, in the series described in supplementary informations section 2 (figure S2, panel c), three samples show no noticeable bulk doping and two samples shows a small bulk p-doping. The large electron and hole mobilities, $\mu_e \simeq 110 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $\mu_h \simeq 40 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, secure a GHz bandwidth

in our ten-micrometer-long n-MOSFETs suited for IR sensing. The capacitance-voltage $C_G(V_G)$ dependence confirms the MOSFET inversion-depletion-accumulation regimes and allows measuring the depletion-layer thickness $\delta_{dep.} \simeq 15$ nm. This value puts on quantitative basis the above distinction between 2D-FETs and MOSFETs based on DC transport. Finally the potential of PdSe₂-MOSFETs for fast infrared detection is discussed.

II. DEVICE FABRICATION AND SETUP

PdSe₂ transistors are fabricated by exfoliating high-quality PdSe₂ crystals [4] grown by a self-flux method as described in Ref.[4], and transferring them onto large hBN flakes, exfoliated from high-quality hBN crystals grown under high pressure-high temperature as described in Ref. [20] acting as bottom-gate dielectric. Incipient to the stamping technique, the hBN thickness varies from device to device as specified in the supplementary informations (table 1 in section SI 2). Transistors are deposited on a gold bottom gate itself evaporated on SiO₂ substrate. They are embedded in 50 Ω coplanar wave guides (CPW) used for DC and RF characterization. Note that this RF-device geometry precludes 4-terminal DC transport measurement and direct separation of channel and contact resistance. PdSe₂ samples are chemically etched to the final rectangular dimensions (length $L \lesssim 10 \ \mu m$ and width $W \gtrsim 10 \ \mu m$) and equipped with low-resistance palladium (Pd) contacts using laser lithography and deposition. The bottom gate is made of gold, which has a work function $(\mathcal{W}_{Au} = 5.3 \pm 0.2 \text{ eV})$ close to that of Pd contacts $(\mathcal{W}_{Pd} = 5.4 \pm 0.2 \text{ eV})$ [24] and of PdSe₂ valence band edge ($\mathcal{W}_{PdSe_2} = 5.4 \text{ eV}$) [3,25]. Devices show a year-long stability, in spite of the absence of top capping. PdSe₂ structural quality is assessed by Raman spectroscopy, exemplified in Fig.SI1-a, with peaks associated with optical phonon inelastic scattering at $\hbar\Omega_{OP} \simeq 145 \text{ cm}^{-1} = 18 \text{ meV} [4,5,26].$

We have investigated two series of transistors qualified as thin $(t_{PdSe_2} \lesssim 20 \text{ nm})$ and thick $(t_{PdSe_2} \gtrsim 90 \text{ nm})$. We focus here on one representative thick device (sample S43) shown in the inset of Fig.1-(a), with $t_{PdSe_2} = 90 \text{ nm}$ $(t_{hBN} = 34 \text{ nm})$. Statistical relevance of S43 is illustrated in Figs.SI2-(a-d) according to the room-temperature transfer characteristics and typical RF admittance spectra of the thick device series. For comparison, we show in the inset of Fig.1-(b) one representative thin device (sample S02) with $t_{PdSe_2} = 9 \text{ nm}$ $(t_{hBN} = 47 \text{ nm})$. Their micrometer sizes, specified in the caption of Fig.1,



FIG. 1: Metal-hBN-PdSe₂ field-effect transistors. Optical image of S43 PdSe₂-MOSFET (Fig.1a left inset with $L \times W = 10 \times 25.5 \ \mu m$, $t_{PdSe_2} = 90 \ nm$), and of S02 PdSe₂ 2D-FET (Fig.1b inset with $L \times W = 2.8 \times 13.2 \ \mu m$, $t_{PdSe_2} = 9 \ nm$). Main panels of Fig.1a and Fig.1b show the gate voltage dependence of their drain-source resistance at different temperatures. A strong Schottky-barrier (SB) develops in the electron-doped regime of S43 at low temperature; its activation process is analyzed in Fig.1c with a Richardson law model (dotted-lines, see main text). The extracted SB-height is plotted in Fig.1c (inset); it shows the good work function alignment between metallic Pd and the PdSe₂ valence band edge in the p-doped regime and a plateau in the n-doped regime. The difference gives an SB estimate of the PdSe₂ bandgap $\Delta_{SB} \simeq 0.14 \ eV$. A second estimate is provided by the thermal activation analysis of S43 bulk resistance, measured at surface depletion for $V_G = -1.6 \ V$ in the temperature range $T = 176-300 \ K$ (right-inset in Fig.1a), using the law $RT^{3/2} = A \exp -(\Delta_{bulk}/2k_BT)$ (dashed line); it gives a bandgap $\Delta_{bulk} \simeq 0.15 \ eV$.

match IR wavelengths. Devices are characterized in a cryogenic DC-40 GHz probe station,

their RF scattering parameters being measured over a 5-decade (70kHz–40GHz) bandwidth with a vector network analyzer (Anritsu-MS4644B). Thru-lines and dummy structures are used for CPW and stray capacitance de-embedding purposes. From the full set of scattering parameters we extract the device admittance matrix, including the zero-bias gate-source contribution of interest for the physical characterization of MOSFETs [21].

III. DIRECT CURRENT CHARACTERIZATION

As seen in Figs.1-(a,b), S43 and S02 devices show ambipolar transport at room temperature with similar resistances at large (positive and negative) doping, and a resistance maximum at a charge neutrality point (CNP) $V_{CNP} \sim -1$ V. The similarity of resistances in thin (S02) and thick (S43) doped PdSe₂-transistors already suggests prominent screening effects in bulk samples. The temperature-independent CNP shift indicates a small (n-type) bulk doping. The resistance of thin S02 in Fig.1-b eventually saturates at 10 M Ω at channel depletion, due to the limited resolution of our setup.

The overall shapes of the transfer characteristics of S43 are qualitatively different. They show plateaus at positive gate voltage and low temperature (Fig.1-a) that we attribute to the buildup of a Schottky barrier at the PdSe₂-Pd interface due to work function mismatch between the Pd contact and the conduction band of PdSe₂. This barrier is elusive at negative gate voltage, confirming the good alignment between the Γ bands of metallic Pd and bulk PdSe₂. The same trend is observed for the 2D-FET S02 in Fig.1-b albeit SB-resistance effects being obscured by a larger channel contribution. The transfer characteristic of S43 also shows a maximum at $V_g \simeq -1.6$ V for $T \gtrsim 150$ K, signaling the suppression of surface transport at surface charge neutrality, its temperature dependence is used below to estimate the bulk bandgap of PdSe₂. Below 150 K the Schottky contact resistance dominates over bulk resistance (see the 130 K curve in Fig1.a), blurring the resistance maximum and precluding its quantitative analysis in terms of bulk thermal activation.

To quantify SB effects in S43, we show in Fig.1-c an activation plot together with high-temperature fits (dashed lines) with the Richardson law [27] :

$$R \times T = \frac{4\pi^2 \hbar^3}{e^2 k_B m_e^* \mathcal{A} D} \, \exp \frac{\Phi}{k_B T} \tag{1}$$

where Φ the Schottky barrier height, \mathcal{A} an effective contact area, and D < 1 an electronic

transmission factor accounting for wave-function mismatch between metallic Pd and PdSe₂. Note that a factor 2 has been introduced for the additive source and drain contributions. As seen in Fig.1-c, the resistance obeys Eq.(1) above 100 K and saturates below presumably due to quantum tunneling. The high-temperature extrapolate, $\ln (R_{[k\Omega]}T_{[K]}) \sim 13$ (at $V_G =$ +10 V), agrees with the prefactor in Eq.(1) taking $\mathcal{A} \sim 0.1 \ \mu\text{m}^2$ and $D \sim 0.01$. From the slope we extract $\Phi(V_g)$, plotted in the inset of Fig.1-c, which shows a stepwise increase from $\Phi_{inv} \simeq -0.02$ eV in the inversion regime to $\Phi_{acc} \simeq +0.15 \pm 0.01$ eV in the accumulation regime (blue squares). The small negative Schottky barrier extracted is physically irrelevant and discloses the absence of Schottky barrier between metallic Pd and p – PdSe₂. From the sum $\Phi_{acc} + \Phi_{inv}$ we infer a first estimate of PdSe₂ bandgap: $\Delta_{SB} \sim (\Phi_{acc} + \Phi_{inv}) \simeq$ 0.15 ± 0.01 eV.

We have also performed an analysis of activated transport at depletion $(V_g \simeq -1.6 \text{ V})$ using the standard law for intrinsic bulk semiconductors, $RT^{3/2} = A \exp{-(\Delta_{bulk}/2k_BT)}$. The analysis is limited to a reduced temperature range T = 150-300 K where a the resistance peak at surface charge neutrality is visible, securing a negligible contribution of contact Schottky barrier effects. We deduce an estimate of the bandgap $\Delta_{bulk} = 0.15 \text{ eV}$. A similar analysis performed on S02 yields a somewhat larger $\Delta_{bulk} \simeq 0.3 \text{ eV}$. Both values remain below the theoretical expectation $\Delta \simeq 1.3 \text{ eV}$ for single layer PdSe₂. Based on these two independent determinations, we conclude that transport bandgap of semi-bulk PdSe₂ does not completely vanish but rather saturates at $\Delta_{PdSe_2} = 0.15 \text{ eV}$, consistently with theoretical prediction in Ref.[4]. Note that while the SB is used here for bandgap characterization purpose, it can be minimized by appropriate contact engineering [28] for applications.

IV. HIGH-FREQUENCY GATE CAPACITANCE SPECTROSCOPY

Field-effect capacitance is a well established characterization technique of semiconductor devices [18]. It can be indifferently performed in capacitors (MOSCAPs) or transistors (MOSFETs). MOSCAPs are commonly made of silicon [29], or narrow-bandgap InAs [30] semiconductors, with a top gate and a thin oxide insulator, distinctively called MOS devices. The gate capacitance is generally measured between the top gate and the (weakly) doped bulk. Here we use an in-plane variant, introduced for graphene [21], and used in high mobility hBN encapsulated graphene devices including plasma-resonant capacitors [31], which



FIG. 2: Zero bias gate admittance spectra $\mathcal{I}[Y_{GS}](f)$ (blue circles) and $\mathcal{R}[Y_{GS}](f)$ (red squares) of PdSe₂-MOSFET-S43 at T = 176 K (Figs2.a,c) and T = 294 K (Figs2.d,f). These typical spectra correspond to inversion (a,d), depletion (b,e) and accumulation (c-f) regimes. Solid lines are fits to Eq.(2) according to the lumped element circuit sketched in Fig.2-b which includes : the resistance $r = R/L = 1/\sigma W$ and capacitance $c_Q = C_Q/W$, the hBN insulator capacitance $c_{hBN} = C_{hBN}/W$, and the Schottky-contact resistance R_{SB} and capacitance $C_{SB} \sim 30$ fF, corresponding to a Schottky surface capacitance of the Pd/n – PdSe₂ interface on the order of $c_{SB} \sim 1$ fF/ μ m². Spectra show a crossover at $f_{ew} \sim 0.1$ –10 GHz between a capacitive regime, $\mathcal{R}[Y_{GS}] \propto f^2 \ll$ $\mathcal{I}[Y_{GS}] \simeq 2\pi f C_G$, and an evanescent wave regime, $\mathcal{R}[Y_{GS}] \simeq \mathcal{I}[Y_{GS}] \propto \sqrt{f}$. The SB contribution appears as a low-frequency crossover at $f_{SB} \sim 1/R_{SB}C_{SB} \sim 10$ MHz in Fig.2-c.

takes into account the Schottky contact impedance. It has also been exploited to characterize the topological Dirac states at the surface of Bi2Se3-tetradymites [34], as well as the interface states of topological heterojunctions between normal and inverted HgTe/CdHgTe

semiconductors [32], and the edge states of strained HgTe quantum wells [33]. The complex gate-source admittance is measured over a broad frequency range allowing for a combined in-situ characterization of gate capacitance $C_G(V_G)$ and channel conductivity $\sigma(V_G)$. The admittance spectrum reflects a crossover from an elastance $(1/C_G)$ dominated regime at low frequency to a lattice-friction dominated regime at high frequency. Such an RF crossover from elastic-dominated to friction-dominated response is quite general and has been previously reported in the context of vortex matter dynamics in superconductors [36-38]. In atomically thin 2D materials, screening is negligible and one can readily extract from $C_{\rm G}$ the quantum compressibility contribution $C_Q = e^2 DOS$ in series with the geometrical capacitance C_{geo} . This provides in turn a determination of the chemical potential $E_F = \int (C_G/C_{qeo} - 1) dV_q$ and the diffusion constant $\mathcal{D} = \sigma/C_Q$, yielding a genuine scattering spectroscopy encoded in the $\mathcal{D}(E_F)$ dependence [32]. For massive PdSe₂ carriers, the 2D density of states in the surface layer, $DOS = m^*/\pi\hbar^2 \sim 10^{14} \text{ cm}^{-2}/\text{eV}$, is large such that $C_Q \gg C_{geo}$, and the gatevoltage dependence of C_G mostly stems from series dielectric channel contributions. These contributions read $C_{\text{PdSe}_2} \approx \epsilon_{\text{PdSe}_2} / \delta_{dep/inv}$, with δ_{dep} the depletion-layer depth at neutrality, and δ_{inv} that of the p⁺-n junction in the inversion regime.

Figure 2 shows typical RF gate-admittance spectra $Y_{GS}(\omega)$ of PdSe₂ n-MOSFET S43 at room temperature T = 294 K (d-f) and low temperature T = 176 K (a,c). Negative and positive gate voltages correspond to (hole) inversion and (electron) accumulation regimes. A room-temperature depletion spectrum, for $V_g \sim -1$ V, is shown in panel (e). Also shown in the figures are theoretical fits with a 1D charge diffusion model [21,33] based on a lumpedelement description (sketched in Fig.2-b):

$$Y_{GS}(\omega) = \frac{1 - e^{-\gamma L}}{Z_D + Z_0} \frac{1 + \Gamma_S \exp{-\gamma L}}{1 - \Gamma_D \Gamma_S \exp{-2\gamma L}},$$
(2)

where $Z_0 = \sqrt{\frac{r}{jc_g\omega}}$ and $\gamma = \sqrt{jrc_g\omega}$ are the line impedance and propagation constant respectively, with r = R/L and $c_g = C_g/L$ the resistance and gate capacitance per unit length. Z_S and Z_D are the source and drain contact impedance, and $\Gamma_D = \frac{Z_D - Z_0}{Z_D + Z_0} \Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}$ are the reflection coefficients at the drain and source contact respectively. The contact impedance is modeled as $Z_{SB} = (R_{SB}^{-1} + jC_{SB}\omega)^{-1}$ and the channel conductivity is $\sigma = (rW)^{-1}$. Data being measured in a transistor geometry, the gate admittance is the sum of the gate-source and gate-drain contributions which are nominally equal at zero drain-source bias; hence the factor 2 in Eq.(2) and a factor 1/2 in that of k. As seen in Figs.2-(a,c-f), the 1D-model (solid lines) captures well the 4-decades admittance spectra, both at room temperature (d-f) and in the inversion/accumulation regimes at low temperature (a,c). It fails describing the low-T depletion regime in Fig.2-b when both surface-layer and bulk transport are suppressed. Similarly, it also fails describing S02 admittance spectra (not shown). The 1D response is characterized by a crossover frequency $f_{ew}(V_G) \sim 1$ GHz between a low-frequency capacitive regime, $\mathcal{I}(Y_{GS}) \propto f$ and $\mathcal{R}(Y_{GS}) \propto f^2$, and a highfrequency regime, $\mathcal{R}(Y_{GS}) \simeq \mathcal{I}(Y_{GS}) \propto f^{1/2}$, which is characteristic of evanescent waves in diffusive media. In the depletion regime (Fig.2-e), f_{ew} drops to a finite 0.1 GHz value controlled by the small, thermally activated, bulk conduction. The transport crossover frequency f_{ew} acts as an optical cutoff frequency for photo-transistors above which photocarrier detection is limited to the very vicinity of contacts, within a length $k^{-1} \ll L$.



FIG. 3: Gate voltage dependence of channel conductance σ and capacitance C_G deduced from RF gate capacitance spectroscopy in Fig.2. The inverse capacitance (called elastance) obeys $C_G^{-1}(V_G) = C_{hBN}^{-1} + C_{PdSe_2}^{-1}$ (blue symbols), where $C_{hBN} \approx C_{AL} \simeq 0.74 \text{ mFm}^{-2}$ ($\epsilon_{hBN} \simeq 3.2\epsilon_0$) is the hBN dielectric contribution. Note that 294K elastance data have been down shifted by 0.25 m²/mF for clarity. The elastance step between accumulation and depletion regimes measures the chargedepletion depth (see main text). Blue dashed and dotted lines are empirical fits used to extrapolate the depletion capacitance value. The conductivity $\sigma(V_G)$ (red symbols) reveals the ambipolar response of the channel. Difference between 294K and 176K data highlights the contribution of bulk thermal carriers and allows extracting T-independent mobilities: $\mu_e \simeq 110 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $\mu_h \simeq 40 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$.

Relying on the quality of the fits (see the supplementary video), we can extract the deembedded contact and channel resistances. In supplementary informations (section 3), they are analyzed using the same Richardson and Arhhenius plot used in DC (see section III). Both analyses confirm a bandgap value of 0.15 eV and the consistency of DC and RF responses.

But we can now push our analysis further, by extracting accurate values of gate capacitance $C_G(V_G)$ and channel resistivity $\sigma^{-1}(V_G)$, as shown in Fig.3. At room temperature, the contact impedance Y_{SB}^{-1} is reduced and Y_{GS} is mostly dominated by the channel contribution. The situation is different at low-temperature, specifically in the accumulation regime $(V_G > 0)$, where contact resistance was shown to be overwhelming at DC (see Fig.1-a). Its signature is a low-frequency deviation from the 1D propagation, below a Schottky-barrier cutoff frequency $f_{SB} \sim 1/R_{SB}C_{SB} \sim 10$ MHz. Above f_{SB} , the large contact resistance $(R_{SB} \sim 1 \text{ M}\Omega)$ is bypassed by the contact capacitance $(C_{SB} \sim 30 \text{ fF})$ and one recovers a diffusive channel admittance response. A proper account of R_{SB} and C_{SB} in Eq.(2) allows extracting reliable values of C_G and σ . By deembedding contact contributions, Fig.3 illustrates the temperature effect on the channel elastance $1/C_G = 1/C_{hBN} + 1/C_{PdSe_2}(V_G)$ and the ambipolar conductivity.

Let us focus first on the room-temperature data (empty symbols) in Fig.3. Channel conductivity (empty red squares) depicts, with an enhanced precision compared to the DC data in Fig.1-a, the ambipolar character and the strong gate modulation of the PdSe₂-MOSFET. It peaks at $\sigma^{-1} \simeq 280 \text{ k}\Omega$ in the depletion regime ($V_g \simeq -0.7 \text{ V}$), and drops down to $\sigma^{-1} \simeq 5 \text{ k}\Omega$ in the accumulation regime ($V_g = +10 \text{ V}$), and $\sigma^{-1} \simeq 50 \text{ k}\Omega$ in the inversion regime ($V_G = -10 \text{ V}$). Carrier mobility is fair, with $\mu_{acc.} \simeq 110 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $\mu_{inv.} \simeq 40 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, approaching the $\mu \simeq 250 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ value reported in PdSe₂ FETs after annealing [4,5]. Gate elastance (blue circles, note that data are shifted by $-0.25 \text{ m}^2/\text{mF}$ for clarity) is characteristic of n-MOSFETs [18,29,30]: it saturates in the accumulation regime at the (nominal) gate insulator value $C_G \approx C_{hBN} \simeq 0.74 \text{ mF/m}^2$, takes a minimum $C_G \simeq 0.52 \text{ mF/m}^2$ at depletion, and increases to a plateau $C_G \simeq 0.56 \text{ mF/m}^2$ characteristic of an inversion regime [18]. From the additivity of insulator ($1/C_{hBN}$) and semiconductor ($1/C_{PdSe_2}$) elastance contributions, we deduce $C_{PdSe_2} \simeq 1.75 \text{ mF/m}^2$ at depletion and $C_{PdSe_2} \simeq 2 \text{ mF/m}^2$ in the inversion regime. Relying of the theoretical estimate $\epsilon_{PdSe_2} = 3\epsilon_0$ [39], we infer $\delta_{dep} \simeq 15 \text{ nm}$ and $\delta_{inv} \simeq 13 \text{ nm}$. These small screening lengths,

which are consistent with the Debye length $L_D = \sqrt{k_B T \epsilon_{\text{PdSe}_2}/e^2 N_D} \gtrsim 7$ nm for a bulk doping $N_D \lesssim 1 \ 10^{17} \text{ cm}^{-3}$, secure the MOSFET interpretation of our 90 nm-thick S43 device, and justify the qualitative difference between our thin and thick transistor series.

The difference between 294 K and 176 K data in Fig.3 illustrates thermal effects on mobility and carrier density. As expected the capacitance gate modulation is more contrasted at 176 K due to a smaller contribution of the thermal carriers to screening. To quantify the first effect we cannot rely on direct measurement of C_G at depletion due to the above-mentioned poor quality of the fits. Instead, we have used a three-parameters empirical interpolation formula, $C_g^{-1}(V_g) = C_g^{-1}(+10 \text{ V}) - a \tanh\left[(V_g - V_{CNP})/b\right] + c/\sqrt{b^2 + (V_g - V_{CNP})^2}$ where a, b and c encode respectively for the capacitance step between depletion and accumulation, the amplitude and width of the capacitance dip at neutrality. Catching the room temperature $C_G(V_G)$ data (dotted blue line), it is used to fit 176K-data over the inversion/accumulation regimes (dashed blue line). With this procedure we infer $\delta_{inv} \simeq 15$ nm and $\delta_{dep} \simeq 20$ nm at 176 K. Temperature effect on $\sigma(V_G)$ is also instructive: room-temperature data are mainly upshifted by a constant amount $\Delta \sigma \simeq 3 \ \mu S$ with respect to 176-K data, implying that : i) the mobility is essentially T-independent as expected for impurity scattering, and ii) the bulk contribution, which is suppressed at 176 K, is thermally activated at room temperature with a bulk resistivity $t_{\rm PdSe_2}/\Delta\sigma \simeq 3$ Ohm.cm. This value is consistent with a thermal carrier density $n_i(300 \text{K}) \sim 1.10^{17} \text{ cm}^{-3}$ for a bandgap $\Delta_{bulk} = 0.15 \text{ eV}$, and a bulk mobility $\mu_{bulk} \simeq 20 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$. The finite bulk mobility augurs well of a fast bulk-surface dynamics of photo-carriers under illumination as anticipated in the introduction.

V. CONCLUSION

In this letter we have reported on low-bias DC transport and RF gate capacitance spectroscopy in high-quality PdSe₂ crystals providing qualitative and quantitative evidence that semi-bulk van der Waals PdSe₂ transistors behave as genuine narrow-bandgap MOSFETs. This extensive electronic characterization allows down-pinning relevant material parameters such as PdSe₂ work function, transport bandgap, mobility, and thermal carrier density. In particular, we have deduced a fundamental electronic bandgap of 0.15 eV in line with the ab initio studies. [4,6] Our work suggests that the optical gap of 0.5 eV reported in the literature [5,13] originates from higher energy transitions and offers guidance for further infrared opto-

electronic applications. Finite bias properties (not reported here) confirm the quasi-intrinsic quality of our $PdSe_2$ transistors. However they call for a different out-of-equilibrium physics (phonon-induced velocity saturation, self heating, etc..) which is beyond the scope of the present paper.

The demonstration of PdSe₂-MOSFETs opens new perspectives for applications of 2D materials in high-speed optoelectronics including ultra broadband optical detectors covering the mid-infrared range. The present demonstration of GHz electronic bandwidth at the MIR-relevant 10 μ m length scale, put in perspective with literature photo-detection measurements of an optical gain G = 700 A/W [15], opens an avenue to PdSe₂ MOSFETs for room-temperature monolithic broadband and high-speed sensing, competing the extensively used CdHgTe detectors [40].

Acknowledgments

Authors acknowledge fruitful discussions with A. Vasanelli and Y. Guldner and thank M. Pala for proofreading the manuscript before submission. The research leading to these results has received partial funding from the the European Union "Horizon 2020" research and innovation programme under grant agreement No.785219 "Graphene Core", from the ANR-2018-CE08-018-05 "BIRDS". R. Le Goff thanks Thales Systèmes Aéroportés for the CIFRE grant No.2016/1294 funding.

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